The following Listing of Claims replaces all prior versions and listings of claims in this application.

LISTING OF CLAIMS

1.-27. (Canceled)

28. (Previously presented) A multiband Phase-Locked Loop (PLL) arrangement, comprising:

a single-loop PLL including a phase/frequency detector, a loop filter, a Voltage-Controlled Oscillator (VCO), and a reference voltage signal (V_{ref}) input to the arrangement;

a control circuit for locking the VCO to a correct frequency band, the control circuit including a multi-window circuit having at least two amplitude windows, each amplitude window being defined by respective upper and lower voltage levels; and

a comparison device for comparing a VCO control voltage output from the loop filter with the upper and lower voltage levels of an amplitude window;

wherein if the VCO control voltage settles within a first amplitude window, a second narrower amplitude window is selected and the VCO control voltage is compared with the upper and lower voltage levels of the second amplitude window; if the VCO control voltage settles within the second amplitude window or a further subsequent even narrower amplitude window, phase lock is achieved;

if the VCO control voltage does not settle within an amplitude window, the comparison device provides a signal for providing a second control signal to the VCO for switching the VCO to another frequency band; and for the other frequency band, the VCO control voltage signal is compared with at least one of the amplitude windows to determine if phase lock is achieved in the other frequency band.

29. (Previously presented) The arrangement of claim 28, wherein the VCO control voltage comprises an analog signal.

30. (Previously presented) The arrangement of claim 29, wherein the second control signal comprises a digital signal.

31. (Previously presented) The arrangement of claim 30, wherein the comparison device comprises first and second comparators for comparing the VCO control voltage with the upper voltage level and the lower voltage level, respectively,

and if the VCO control voltage exceeds the upper voltage level or is below the lower voltage level, a corresponding signal is provided to a switching enabler to indicate whether a switch is to be done to a higher frequency band or to a lower frequency band.

32. (Previously presented) The arrangement of claim 31, wherein the comparison device is connected to a first delay device such that if a switch is to be done to another frequency band, the corresponding signal is clocked into the switching enabler after lapse of a time period.

33. (Previously presented) The arrangement of claim 32, wherein the switching enabler comprises a state machine that provides the second control signal to the VCO based on the clocked signal from the switching enabler.

34. (Previously presented) The arrangement of claim 28, wherein when phase lock has been achieved, an amplitude window having an arbitrary size can be selected from the amplitude windows available in the multi-window circuit.

35. (Previously presented) The arrangement of claim 28, wherein the control circuit comprises a lock detection circuit for continuously monitoring whether phase lock has been achieved.

36. (Previously presented) The arrangement of claim 35, wherein the lock detection circuit comprises an initializer that restarts the control circuit with the first amplitude window if phase locking is not achieved or if phase lock is lost.

37. (Previously presented) The arrangement of claim 36, wherein the lock detection circuit uses signals output from the comparison device and from the multi-window circuit to establish if the VCO control voltage falls within an amplitude window, such that if the VCO control voltage does not fall within the amplitude window, the initializer restarts the control circuit, otherwise a lock-achieved condition is indicated.

38. (Previously presented) The arrangement of claim 31, further comprising a loop switch arrangement having a threshold circuit for adjusting the VCO control voltage to substantially assume a desired voltage within an amplitude window after frequency band switching.

39. (Previously presented) The arrangement of claim 38, wherein the threshold circuit controls a switching arrangement comprising two transistors for charging or discharging a VCO control voltage control point, depending on whether adjustment of

the VCO control voltage upwards or downwards is needed, using a supply voltage or ground until the VCO control voltage substantially assumes a desired voltage within the amplitude window.

40. (Previously presented) The arrangement of claim 39, wherein signals from the first and second comparators and the VCO control signal are input to the threshold circuit, and the threshold circuit uses the input signals to establish whether adjustment upwards or downwards of the VCO control signal is needed and whether no adjustment is needed.

41. (Previously presented) The arrangement of claim 39, wherein a single supply voltage is used.

42. (Previously presented) The arrangement of claim 28, wherein the single-loop PLL is a narrowband PLL.

43. (Previously presented) The arrangement of claim 34, wherein upon achieving phase lock, an amplitude window larger than a smallest amplitude window within which phase lock was achieved is selected as an operation window.

44. (Previously presented) The arrangement of claim 39, wherein the control point is located in the loop filter.

45. (Previously presented) The arrangement of claim 44, wherein the loop filter is an active filter that includes an amplifier, and the control point is located before the amplifier.

46. (Previously presented) The arrangement of claim 28, wherein the single-loop PLL includes a charge-pump PLL that includes a charge storage device, the VCO control voltage is based on charging and discharging of the charge storage device, and the loop filter is a passive filter.

47. (Previously presented) A method of controlling a multiband phase-locked loop (PLL) arrangement that includes a single-loop PLL having a phase/frequency detector, a loop filter, a Voltage-Controlled Oscillator (VCO), and a reference voltage signal V_{ref} input to the arrangement, the method comprising the steps of:

(a) providing the reference voltage signal V_{ref} to the single-loop PLL and to a multi-window circuit;

(b) setting an amplitude window defined by upper and lower voltage levels in the multi-window circuit;

(c) establishing whether an analog VCO control voltage output from the loop filter settles within the set amplitude window;

(d) if so, setting a narrower amplitude window in the multi-window circuit and establishing if the analog VCO control voltage settles within the narrower window;

(e) if not, using a result of the comparison to establish whether to switch to a higher frequency band or to a lower frequency band;

(f) providing a digital control signal to the VCO to switch the VCO to the higher frequency band or to the lower frequency band; and

repeating steps (a)-(e) unless a frequency band switch is required until phase lock is achieved.

48. (Currently amended) The method of claim 47, further comprising ~~the step of~~ resetting the analog VCO control voltage when there is a switch of frequency band.

49. (Currently amended) The method of claim 47, further comprising ~~the step of~~ adjusting the analog VCO control voltage after switching frequency band such that the analog VCO control voltage assumes a desired voltage within an amplitude window based on a digital threshold circuit and a transistor arrangement using a single supply voltage.

50. (Currently amended) The method of claim 47, further comprising ~~the steps of~~:

continuously monitoring whether a phase lock condition has been achieved, and

indicating when phase lock has been achieved in a smallest amplitude window, and

resetting the analog VCO control voltage if the analog VCO control voltage does not settle within an amplitude window.

51. (Currently amended) The method of claim 49, further comprising ~~the step of~~ providing a signal from the transistor arrangement to a control point in the loop filter.

52. (Previously presented) The method of claim 51, wherein the loop filter is an active filter.

53. (Previously presented) The method of claim 52, wherein the control point is located before an amplifier in the loop filter.

54. (Previously presented) The method of claim 47, wherein the analog VCO control voltage is based on charging and discharging a charge storage device in the single-loop PLL.